OPIMISING SNUBBERS FOR HIGH-CURRENT EMITTER-SWITCHED TRANSISTORS

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INTRODUCTION

A high-current cascode-switch for operation at 100A off a rectified 3-phase 415V supply has been developed, and tested at 80A and 600V to show that significant storage-time and turn-off crossover-time improvements are obtained with large-area, 1000V transistors (1). The low crossover-time (<150nS @ 80A,600V) and storage-time (<750nS @ 80A,600V) of emitter-switched large-area transistors makes their application feasible in medium-power (10-100kW) phase-legs, operating at ultrasonic chopping frequencies. Fast switching and enhanced ruggedness at turn-off, considerably reduces the shunt snubbing required. However, reduced current-fall time (≤30nS up to 80A @ 600V, di/dt≤4500A/μs) demands very hard (Lstray <50nH) voltage clamping to uphold transistor Vceo ratings. At high-current (≥80A), when circuit parasitic-inductance and diode forward-recovery (>50v) effects are significant, it is difficult to exploit the power-loss advantage of soft voltage-clamps (fig.1A), and adaptable voltage-clamps become necessary to avoid impractical hardware-layout and complex compensated clamps. Also, emitter switching does not improve transistor turn-on performance. For good transistor utilization, series snubbing is still required to reduce turn-on power-loss or forward-bias second breakdown, and overcome the limited peak/continuous current factors (≤1.5 for Vcex≥1000V) of high-voltage transistors, by limiting freewheel-diode (1000V) recovery current peaks. With little shunt-snubbing, the power-loss in resetting series-snubbers predominates. A significant improvement in power-conversion efficiency would result with non-dissipative reset circuits. The two problems highlighted, high-current hard voltage-clamping and non-dissipative snubber resetting, are now being tackled, but in cascode-switch development, a soft voltage-clamp was used (fig.1A), to reset the series-snubber and hard-clamp the transistor voltage. Despite its limited clamping effectiveness above 80A and inefficiency in snubber resetting, it keeps snubber circuits very simple while developing base and emitter drive circuits. The soft voltage-clamp was therefore analysed to find a simple design procedure for optimising series-snubber and clamp reset-time for a given voltage rise above the supply-rail. This paper presents the analysis. It is applicable to other switches requiring voltage clamping rather than load-line tailoring, particularly MOSFET's; eg. soft voltage-clamps are commonly used in bridges to prevent MOSFET avalanching by unclamped stray inductance, during load-current commutation between MOSFET and freewheel-diode. Their advantages (2) of; reduced power dissipation over shunt-snubbers; current-dependent power dissipation, independent of supply-voltage; and absence of cross-current peaks in phase-legs are likely to promote continued usage.

ANALYSIS OF SOFT VOLTAGE-CLAMP

If transistor turn-off crossover-time is much faster than the reset-time of series-snubber inductance the circuit of fig.1B describes voltage-clamp operation at transistor turn-off. The most important clamp function is constraining collector-voltage overshoot. Very close clamp-diode, clamp-capacitor, and transistor connection is assumed, such that loop Tr,Cc,&Dc inductance is orders of magnitude below other inductances. L3 and L5 represent stray inductance common to loops Cs,R,&Cc and Cs,Ls,Dc,&Cc. By close connection of Cc and Cs, and by taking a separate connection from R to Cs, L5 is reduced at the expense of L3 and L4, and fig.1C results. Stray inductance L7 enhances series-snubber action and adds to Ls to form L1. Inductance L6 adds to resistor parasitic inductance L4 to form L2. Also, Cs is normally far greater than Cc, and capacitor C in fig.1D is given value Cc. Note that voltage rises on C obtained by fig.1D are superimposed on the dc-rail voltage, Edc. Initially, for insight into the affect of component values on circuit operation, L2 is assumed negligible. Appendix 1 gives the normalised state-equations for fig.1D. At transistor turn-off (t=0) L1 carries Io. Vc and iL1 are described by the equations of a damped parallel-resonant circuit, until Dc ceases conduction, after which C is discharged exponentially by R. Important parameters are: maximum transistor voltage, set by Edc plus peak capacitor voltage, Vcp; minimum off-time, set by iL1 fall-time, tri; and minimum on-time, set by Vc fall-time, (trv-tri). Figures 2 & 3 show voltage-waveform dependence on damping-factor, ζp. A curve of all peak-voltage values is also given in fig.2. It is apparent that low ζp give low trin values, but high trvn values; and high ζp values give low peak capacitor-voltage, Vcpn, but high trin and trvn values because of exponential tailing. trvn has an optimum value at $0.5<\zeta p<1.0$, see fig.6. These trends are more evident in fig.4 & 5, where Vcpn, and trin & trvn for 90,95,and 99% current and voltage falls versus ζp are given. The degree of exponential-tailing is related to vertical contour-separation. An optimum ζp value exists, which gives the best mix of Vcpn, trin and trvn values when all have to be minimised. Exact values for the optimum ζp for all %-fall contours are given in Table-1. Appendix-1 gives normalisation bases. At low current or switching-

TABLE 1

%-Fall	ζp	Vcpn	trin	trvn
1	0.75	0.41	3.52	5.45
5	0.70	0.46	2.90	4.34
10	0.65	0.48	2.49	3.85

frequency, when resistor inductance is insignificant, fig.4 & 5 are adequate for soft voltage-clamp design (Appendix-2). At low switching-frequency, relaxed trn constraints may apply because of their reduced influence on output-voltage dynamic range. Here, sizing the capacitor value by equating $1/2LI^2$ & $1/2CV^2$ and adding a resistor giving an appropriate discharge time-constant (Appendix-2), will give an oversized capacitor value. The discrepancy between expected and actual Vcp, tri and trv would necessitate considerable empirical re-adjustment as Table-2 shows. Row-1 gives expected values and row-2 gives likely values using crude design. The significant effect of the clamp resistor, effectively in parallel with the capacitor, has been ignored.

TABLE 2

	C(μF)	R(Ω)	Vcp(V)	tri(μS)	trv(μS)
CRUDE APPRX	2.2	1.0	≈150	≈5	≈5
GRAPHS DSGN	2.2	1.0	61.7	10.6	24.1
GRAPHS DSGN L2n=0	0.5	2.4	150	2.5	3.9
GRAPHS DSGN L2n=0.5	1.0	2.5	150	4.0	8.1

CLAMP DESIGN WHEN L2 IS SIGNIFICANT

At high chopping-frequency, resistor and wiring inductance, L2, cannot be ignored. Aluminium-clad 50W resistors have about 0.6µH, 1.3µH and 3µH at 1, 2.2 and 30Ω and connection-loop inductance may add several hundred nH. An increase in clamp-capacitor peak-voltage results, see fig.7 (L2n=L2/L1): the 5% trin and trvn curves are for the L2n=0 circuit. To understand waveform variation with L2n, waveforms produced at L2n-contour intersections with lines of constant Vcpn, line-A; constant ζp, line-B; and constant ζs, line-C (fig.7) are drawn. Figures 8 and 9 show that optimum current and voltage waveforms are obtained near L2n-contour intersection with contour ζs=0.8. Current and voltage waveforms are given in fig.10 for L2n-contour intersections along the ζs=0.8 contour. Figure 11 gives waveforms for points on the L2n=0 contour with the same damping factors, ζp, as fig.10. Waveforms in fig.10 approximate more closely to the desired half-sinewave voltages and quarter-sinewave currents. Plotting trvn and trin for ζs=0.8 would produce similar curves on fig.7 as the L2n=0 curves shown.

TABLE 3

	Vcpn	ζp	trin	trvn	L2n
min trvn	0.61	0.58	2.4	3.5	0.3
best mix	0.69	0.44	1.8	3.6	0.5

The minimum trvn value occurs near the intersection of ζs=0.8 and L2n=0.3 curves in fig.7. Row-1 of Table-3 gives circuit performance. A better compromise between trin and trvn exists at the ζs=0.8 and L2n=0.5 intersection, see Table-3 row-2. Here, trin is reduced by raising trvn, but equal minimum on and off times are obtained. The increased Vcpn necessitates 30% more capacitance according to equ.1.

$$C_2 / C_1 \propto (V_{cpn2} / V_{cpn1})^2 \qquad (1)$$

Appendix-2 gives the initial selection procedure for R, C, and L2. Table-2 gives the results of all the appendix-2 examples for comparison. To conclude; the ostensibly troublesome parasitic resistor and connection inductance, which increases the clamp capacitance required, can by itself, or with added inductance, improve inductor reset-time and clamp reset-time. ζp may be set to lower values than with L2n=0 designs for improved trin, because L2n is effective in reducing the capacitor-voltage exponential-tail. For a more comprehensive soft voltage-clamp design-aid further ζs contours should be added to fig.7, together with voltage and current fall-time curves for circuit conditions along these.

REFERENCES

1. Robinson,F.V.P. and Williams,B.W., "Emitter switching high power transistors", EPE, Sept1987, pp57-59.

2. McMurray,W.M.,"Optimum snubbers for power semiconductors", IEEE Trans.,Vol.1A,No.5, Sept1972, pp593-600.

APPENDIX 1

Normalised parameters for state equations.

$tn = \omega o\, t$ where $\omega o = 1/\sqrt{(L1\ C)}$
$iLn = iLn$ where $Io = iL1(0)$
$Vcn = Vc/Vo$ where $Vo = Io\sqrt{(L1/C)}$
$L2n = L2/L1$

Vcpn = peak capacitor-voltage reached
trin = current, iL1, fall-time or L1 reset-time
trvn = total L1 and C reset-time

minimum transistor off-time ≥ trin
minimum transistor on-time ≥ (trvn - trin)

Other parameter definitions

$\zeta p = (\ 1/(2\ R)\ )\sqrt{(L1/C)}$ damping factor when L2=0
$\zeta s = (\ R/2\ )\sqrt{(C/L2)}$ damping factor when L1 o/c
$\zeta s = 1\ /\ (\ 4\ \zeta p\ \sqrt{L2n}\ )$

Normalised state equations

For L2n = 0	For L2n > 0
$\frac{dVcn}{dtn} = -2\ \zeta p\ Vcn - iLn$	$\frac{dVcn}{dtn} = -iLn - iRn$
$\frac{diLn}{dtn} = Vcn$	$\frac{diLn}{dtn} = Vcn$
	$\frac{diRn}{dtn} = \frac{Vcn}{L2n} - \frac{iRn}{L2n\ \zeta p}$
Analysed using closed form solutions.	Analysed using numerical numerical integration.

APPENDIX 2

Example-1 Result of crude design

Set C and R under the following circuit conditions:
Io = 100A
L1 = 5µH
L2n = 0
tri = 5µS
trv = 10µS

Using $1/2\ C\ Vcp^2 \approx 1/2\ L1\ Io^2$ C = 2.2µF
For Vc < 10% $trv \approx 2.3\ RC$ R = 1.0Ω

Performance using graphs with crude design components

$\zeta p = (\ 1/(2R)\ )\ \sqrt{(L1/C)}$ gives $\zeta p = 0.75$
$\omega o \approx 1/\sqrt{(L1\ C)}$ " $\omega o \approx 0.3 \times 10^6$ rad/s
$Vo \approx Io\sqrt{(L1/C)}$ " Vo =150V

From fig.4 & 5 Vcpn = 0.41 => Vcp = 61.7V
trin = 3.2 => tri = 10.6µS
trvn = 7.2 => trv = 24.1µs

Example-2 Design using graphs when L2n = 0

Set R and C for circuit conditions in Example-1
From Table-1 using 10%-fall curves ζp = 0.65
Vcpn = 0.48
trin = 2.49
trvn = 3.85

$Vcpn = Vcp\ /\ (\ Io\sqrt{(L1/C)}\ )$ gives C = 0.5µF
$\zeta p = (\ 1/(2R)\ )\ \sqrt{(L1/C)}$ " R = 2.4Ω
$trin = \omega o\ tri$ " tri = 3.9µs
$trvn = \omega o\ trv$ " trv = 6.1µs
Component values may be further manipulated to obtain the nearest preferred values. Once Vcpn set by new C value, revised value of corresponding ζp will set trin and trvn on fig. 4 & 5.

Example-3 Design using graphs when L2n = 0.5

Set R, C and L2 for circuit conditions in Example-1. Fig.10 shows that a good compromise between trin and trvn exists at the intersection of contours:
L2n = 0.5
ζs = 0.8
Figure 10 gives trin = 1.8
trvn = 3.6
Figure.7 gives Vcpn = 0.69
ζp = 0.44

$Vcpn = Vcp\ /\ (\ Io\sqrt{(L1/C)}\ )$ gives C = 1.0µF
$\zeta p = (\ 1\ /(2R)\ )\sqrt{(L1/C)}$ " R = 2.5Ω
$trin = \omega o\ tri$ " tri = 4.0µS
$trvn = \omega o\ trv$ " trv = 8.1µS
$L2n = L2\ /\ L1$ " L2 = 2.5µH
Salient values from all the examples given are summarised in Table-2 for comparison.

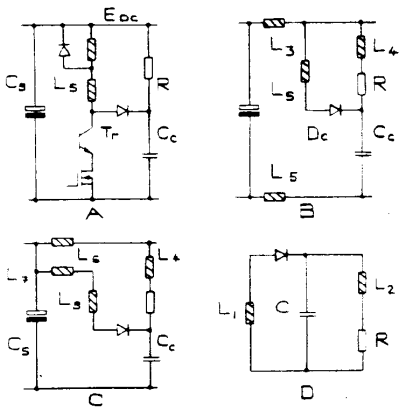


FIG.1 REDUCTION OF SOFT VOLTAGE-CLAMP TO A SIMPLIFIED EQUIVALENT-CIRCUIT

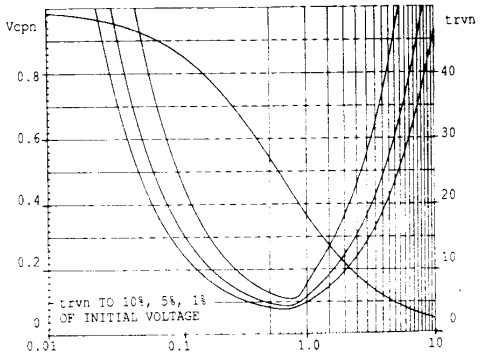


FIG.4 PEAK CAPACITOR-VOLTAGE & DURATION OF VOLTAGE CHANGE, trvn, VERSUS DAMPING-FACTOR

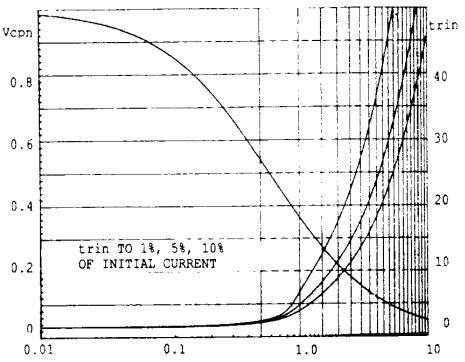


FIG.5 PEAK CAPACITOR-VOLTAGE & SERIES-SNUBBER CURRENT FALL-TIME, trin, VERSUS DAMPING-FACTOR

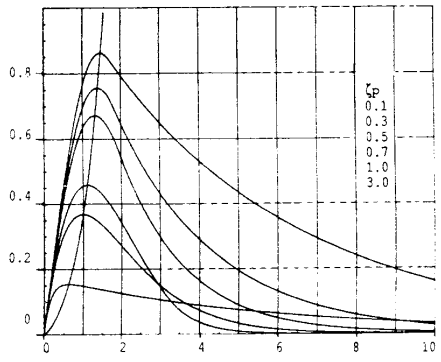


FIG.2 CAPACITOR-VOLTAGE WAVEFORM VARIATION WITH DAMPING-FACTOR, ζp

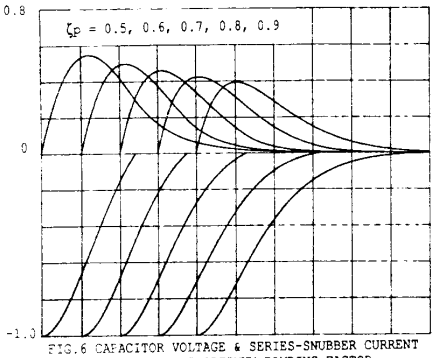


FIG.6 CAPACITOR VOLTAGE & SERIES-SNUBBER CURRENT WAVEFORMS ABOUT THE OPTIMUM DAMPING-FACTOR

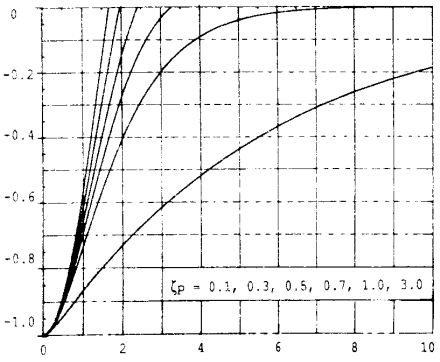


FIG.3 SERIES-SNUBBER CURRENT-WAVEFORM VARIATION WITH DAMPING-FACTOR, ζp

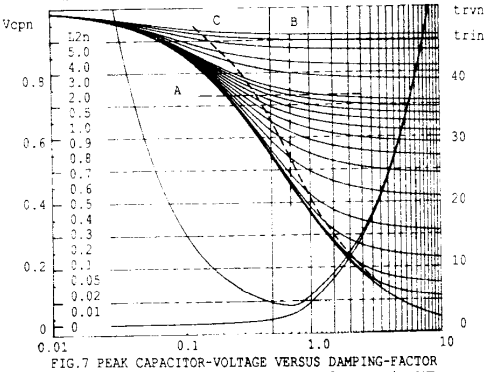
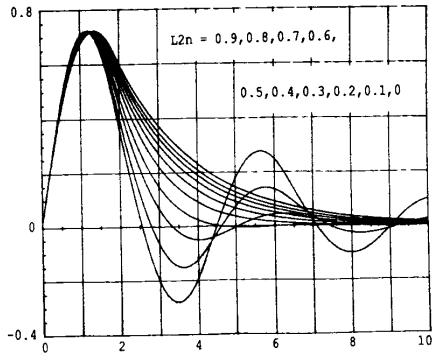


FIG.7 PEAK CAPACITOR-VOLTAGE VERSUS DAMPING-FACTOR FOR DIFFERENT RESISTOR INDUCTANCE, L2n, & trin AND trvn CURVES FOR 95% FALL WHEN (L2N = 0)



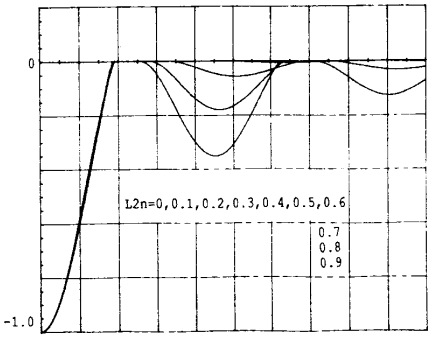
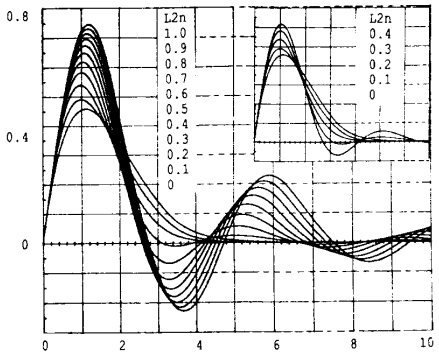


FIG.8 CAPACITOR VOLTAGE & SERIES-SNUBBER CURRENT WAVEFORMS AT L2N-CONTOUR & LINE-A INTERSECTIONS



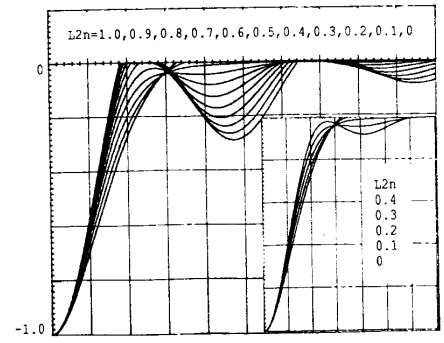
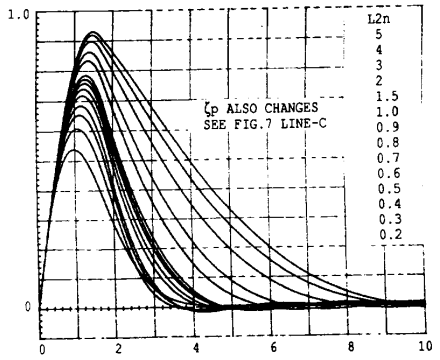


FIG.9 CAPACITOR VOLTAGE & SERIES-SNUBBER CURRENT WAVEFORMS AT L2N-CONTOUR & LINE-B INTERSECTIONS



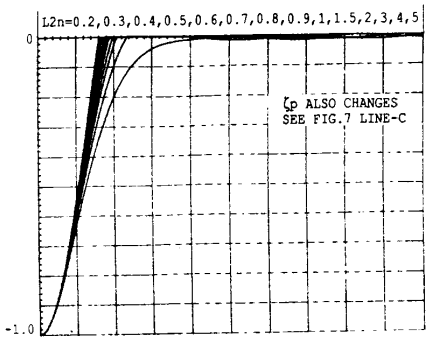
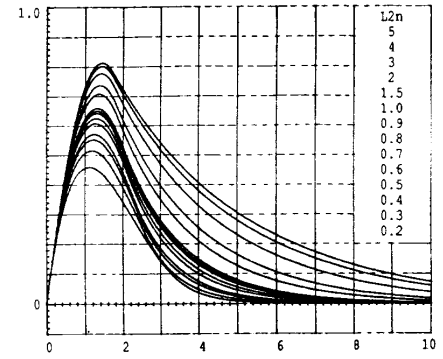


FIG.10 CAPACITOR VOLTAGE & SERIES-SNUBBER CURRENT WAVEFORMS AT L2N-CONTOUR & LINE-C INTERSECTIONS



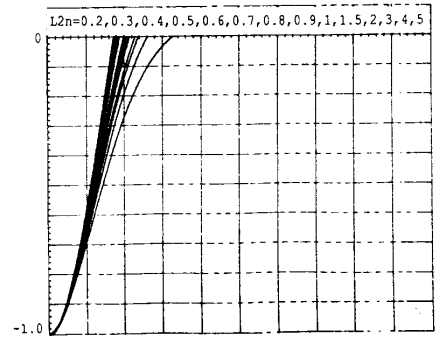


FIG.11 CAPACITOR VOLTAGE & SERIES-SNUBBER CURRENT WAVEFORMS AT POINTS ON (L2N = 0) CONTOUR WITH SAME DAMPING-FACTOR AS L2N-CONTOUR & LINE-C INTERSECTIONS